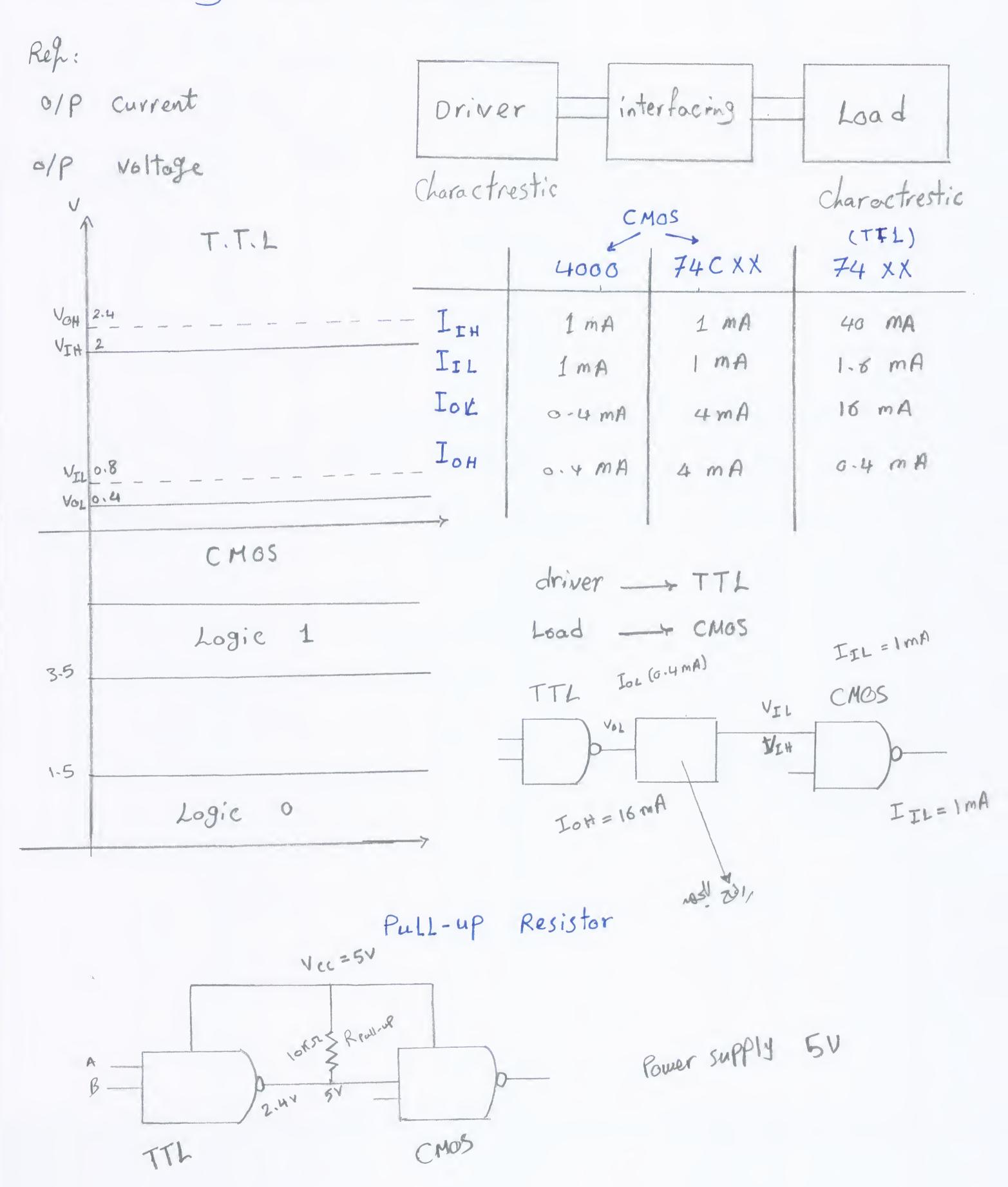
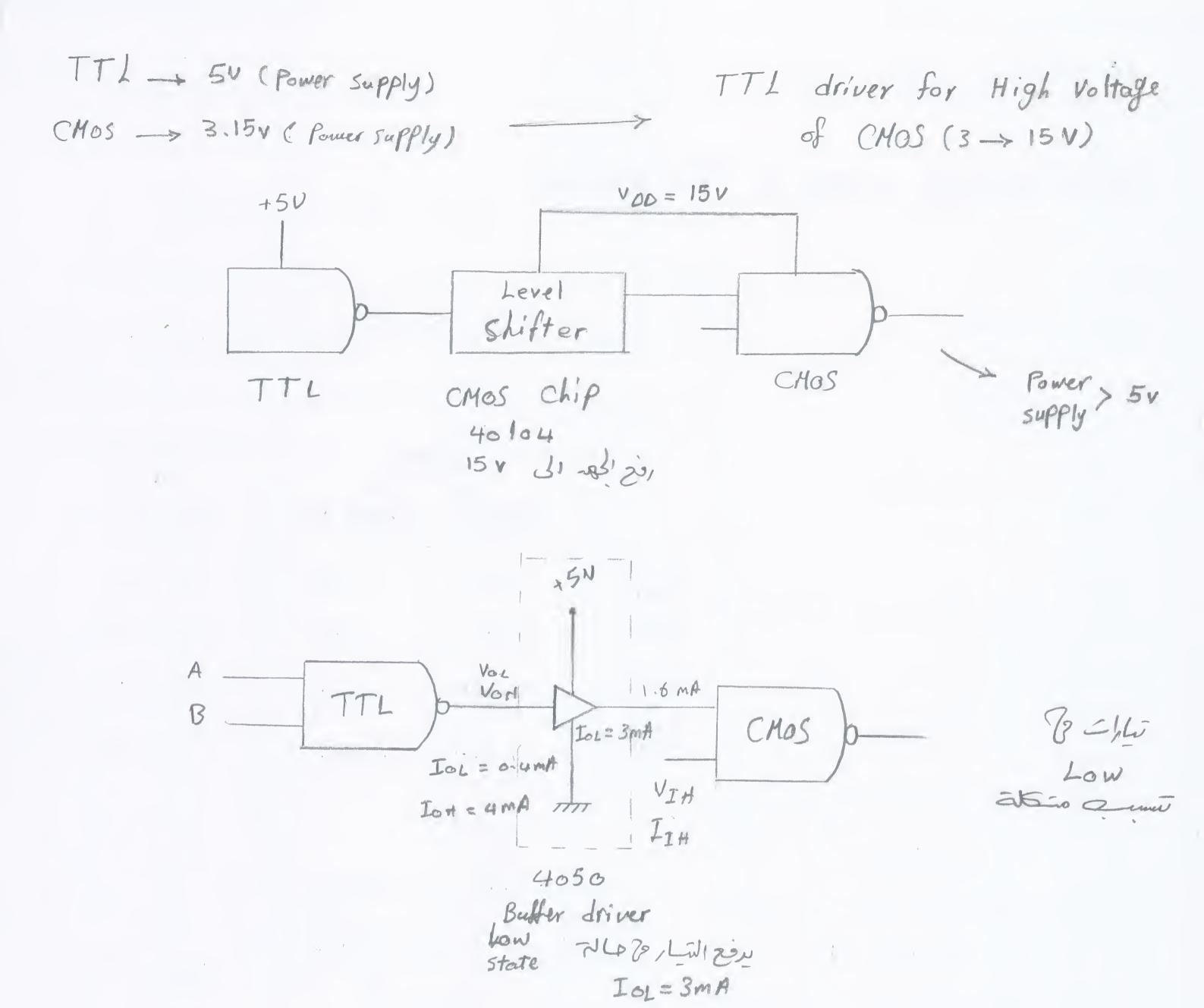
## Interfaceing CMOS & TIL families





## Emitter Coupled Lagic (E.C.L)

\* very fast Than T.T.L Tpd < 1,5 0.8 ns \* Power supply (-) - Hard to interface - used in main Frame Coupler Vccc = OV Pd = 40 mW min Lower diss 220 52 Logic a Vo < - 1.7 V 78052 Vcc = - 5,2 V Vo >, -0.8 V Logic 1 (OR/NOR gate for ECL) A,B (Low state <-1-fv) at -1.3>-1-7 Q-70n Q1, Q2 -> off NB > VE Conduction -> Logic o Q3 -7 00 A, B (High State >, -0.8V) -0.8 > -1-3 Q,, Q2 ->00 out Put VE > VB Q3 -> off (B, , Q2) (@3) Lew LOW

Logic 6

Logie 1